

EXHIBIT A

**REDACTED VERSION OF DOCUMENT
SOUGHT TO BE SEALED**

ATTACHMENT A
EXPERT DISCLOSURE OF TERRENCE DALY AND
EXHIBITS 1-4 THERETO

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Introduction

The United States (the **government**) hereby provides notice of its intent to introduce expert testimony at trial in its case in chief from Terrence (Terry) Daly under Rules 702, 703, and/or 705 of the Federal Rules of Evidence. This disclosure is made pursuant to Rule 16(a)(1)(G) of the Federal Rules of Criminal Procedure.

Witness' Qualifications

Terry Daly is a 35-year veteran of the semiconductor industry. He was formerly senior vice president at GLOBALFOUNDRIES Inc. (**GLOBALFOUNDRIES**), a global semiconductor manufacturing firm (**a foundry**) based in Silicon Valley. At GLOBALFOUNDRIES (2010-2016), Mr. Daly served as head of strategy and corporate development, chief of staff to the CEO, and head of corporate program management. Mr. Daly helped establish a strategic alliance on advanced technology with Samsung and acquire IBM's microelectronics business.

Mr. Daly joined GLOBALFOUNDRIES in 2010 after a 26-year career at IBM (1984-2010). Over the course of his IBM career, he served in financial controller, pricing, and business analysis positions, and held executive roles in manufacturing operations, program management, and strategy. Before joining IBM, Mr. Daly spent five years (1977-1982) as an active-duty officer in the United States Army.

Mr. Daly is a Distinguished Graduate with a bachelor's degree in engineering from the U.S. Military Academy at West Point (1977) and holds a master's degree in international relations from the Fletcher School of Law and Diplomacy, Tufts University (1984).

Currently (2017-present), Mr. Daly is Senior Fellow on the Council on Emerging Market Enterprises (CEME) at the Fletcher School, a multi-disciplinary think tank that studies the intersection of the digital economy and country economic progress across the globe. The focus of Mr. Daly's research is the intersection of policy and technology in U.S. relations with emerging markets, with a special focus on the semiconductor industry, the People's Republic of China, and India. Mr. Daly also provides independent management consulting services in the semiconductor industry.

Engagement Terms and Information Considered

Mr. Daly's hourly rate is \$350.

Exhibit 1 is a list of documents considered by Mr. Daly in this matter in addition to those referenced in this disclosure. Mr. Daly had access to all documents exchanged in discovery in this matter. Because United Microelectronics Corporation, Inc. (**UMC**) continues to produce documents as of the date of this disclosure, Mr. Daly will continue to review documents. The government will supplement this disclosure if additional documents inform Mr. Daly's opinions.

Exhibit 2 is a request for certain documents and information to UMC under paragraph 9 of UMC's plea agreement signed on October 26, 2020.

Exhibit 3 is a summary of the information Mr. Daly received in video conferences with engineers and employees of Micron Technology, Inc. (**MTI**) and Micron Memory Taiwan Co., Ltd. (**MMT**) (collectively, with other MTI subsidiaries and affiliates, **Micron**). Dr. Thomas Dyer, the government's dynamic random access memory (**DRAM**) expert, also attended those video conferences.

Exhibit 4 is a summary of Mr. Daly's video conference with Dr. Dyer.

Mr. Daly will testify that experts in his field would reasonably rely on the foregoing facts and data in forming an opinion on the subjects below.

Subjects of Expert Testimony

Mr. Daly has five principal opinions:

First, modern logic foundries like GLOBALFOUNDRIES and UMC do not make stand-alone DRAM products.

Second, for a foundry independently to develop stand-alone DRAM, the required resources – in money, engineers, and time – vastly exceed those committed by UMC and Fujian Jinhua Integrated Circuit Co., Ltd. (**JHICC**) in those companies' joint technology development program, **Project M**.

Third, although the resources committed to Project M were not sufficient independently to develop DRAM technology, they were consistent with the adoption of DRAM technology from a third party.

Fourth, Project M injured Micron.

Fifth, Project M benefited JHICC and the People's Republic of China.

Principal Opinion 1: Modern Logic Foundries Do Not Make Stand-Alone DRAM Products

Mr. Daly will testify about the structure, value chain, and relationships among players in the semiconductor industry in general and the role, capabilities, and services of logic foundries such as GLOBALFOUNDRIES and UMC in particular. Mr. Daly will contrast foundry and DRAM manufacturers, including their different offerings, business models, and challenges. Among other differences, Mr. Daly will explain that foundries make logic products that can be standard (e.g., Intel or AMD) or application-specific and unique to a particular customer (e.g., Qualcomm, Cisco, Apple, Microsoft), while DRAM is typically a commodity that is designed to an industry standard for many customers. Foundries provide services. DRAM manufacturers produce a product.

Mr. Daly will testify that the three major DRAM manufacturers – Samsung Electronics Co., Ltd. (**Samsung**), SK Hynix Inc. (**SK Hynix**), and Micron – are integrated device manufacturers (**IDMs**), which design and make their own products. By contrast, foundries such as GLOBALFOUNDRIES and UMC provide manufacturing services. Mr. Daly will explain that the DRAM industry consolidated into three major manufacturers because the industry is capital intensive, cyclical, and characterized by periodic imbalances between supply and demand that cause large swings in prices and cash flow that squeezed out players such as Elpida Memory, Inc. (**Elpida**). Micron acquired Elpida out of bankruptcy for approximately \$2.5 billion. At the same time, Micron acquired majority ownership of Rexchip Electronics Corp. (**Rexchip**), which was a joint venture between Elpida (65%) and Powerchip Technology Corp.

(24%). Elpida's 25 nm DRAM technology was made at Elpida's fab in Hiroshima, Japan, which was known as E300, and Rexchip's fab in Taiwan, which was known as R1. After Micron's acquisition, Elpida became known as Micron Memory Japan Ltd. (**MMJ**) and the E300 fab became known as F15. Rexchip became known as MMT and the R1 fab became known as F16.

Mr. Daly will testify that DRAM IDMs are not only integrated, but they also manufacture DRAM only of their own design and, as currently operated, can only manufacture DRAM of their own design. Thus, Samsung can manufacture Samsung DRAM and not SK Hynix or Micron DRAM, SK Hynix can manufacture only SK Hynix DRAM, and Micron can manufacture only Micron DRAM. By contrast, foundries do not design products, they provide contract manufacturing services for products designed by several other companies, their customers, after the development and qualification of foundry technology platforms. Those platforms include the process technology "node" (e.g., 28 nm, 14nm, 7nm); a family of pre-qualified intellectual property (**IP**) building blocks used by product designers; and a set of design tools, known as the process design kit (**PDK**) qualified to a specific process technology node at a specific foundry. In foundries, the PDK is the interface between the customer product designer and the foundry. The PDK is used to describe, precisely, manufacturing process details for engineers. It is a set of files that contain descriptions of the basic building blocks of the process technology that will manufacture the design. Those descriptions are stored in what are known as libraries, design rules, schematics, "**SPICE**" models (Simulation Program with Integrated Circuit Emphasis models), and layouts. Because logic foundries do not manufacture stand-alone DRAM products, their PDKs do not provide the tools a third-party chip designer would need to make stand-alone DRAM products. Because DRAM manufacturers are IDMs, they do not provide PDKs to third-party chip designers. *See, e.g., Ernest Worthmann SEMIENGINEERING "A Guide to Advanced Process Design Kits" (Apr. 14, 2014), <https://semiengineering.com/a-guide-to-advanced-process-design-kits/>.*

Mr. Daly will testify that DRAM is substantially different from logic chips. Functionally, memory devices like DRAM are designed to store electrical data. Logic chips perform diverse functions, including: (1) intensive compute processing and system control (e.g., microprocessors), (2) specialized digital processing (e.g., communications), and (3) processing, converting, and creating analog real-world signals into digital form (e.g., analog-to-digital converter). Mr. Daly will explain that the memory cell and stacked capacitors are unique and critical components of DRAM process technology; that the front end of the DRAM technology is more complex than logic, while the back end of logic technology is typically more complex, with many more levels of metal for effective interconnection of the many layers of the logic design; and that DRAM has many unique technical challenges not found in logic, such as redundancy and repair and partial good chips and binning strategies. Because of the differences between stand-alone DRAM and logic products, the two have become discreet market, product, and manufacturing segments in the semiconductor industry. Accordingly, no modern logic foundry manufactures stand-alone DRAM products and no DRAM IDM manufactures commercial-scale logic products.

For purposes of his testimony, Mr. Daly will discuss modern foundries as dating from around the time of GLOBALFOUNDRIES' creation in 2010. For the years primarily relevant to this matter – specifically, 2015-2018, the world's three leading foundries were (and are) Taiwan Semiconductor Manufacturing Corporation (**TSMC**), GLOBALFOUNDRIES, and UMC, in that order. GLOBALFOUNDRIES and UMC each had about nine percent of the global market share in foundry services. *See, e.g., Rick Shafer & Joshua Buchalter, Oppenheimer & Co., Inc., "Semiconductors: Technology and Market Primer 10.0." (Dec. 7, 2017).*

Principal Opinion 2: for a Foundry Independently to Develop Stand-Alone DRAM Products, the Required Resources Vastly Exceed Project M

Because of the differences in business models and offerings of logic-chip foundries such as UMC, on the one hand, and DRAM IDMs, on the other hand, Mr. Daly will testify that no precedent exists for a foundry to develop stand-alone DRAM technology independently or from scratch and successfully compete in the market. In the last few decades, no new at-scale competitors entered the DRAM market. The latest aspiring entrant is the People's Republic of China (PRC) firm ChangXin Memory Technologies (CXMT). DRAM competitors have exited, gone bankrupt, or been acquired, typically during industry downturns, and the industry has consolidated to the three remaining competitors: Samsung, SK Hynix, and Micron. *See, e.g.*, UMCDOJ-00120684 (Stephen Chen custodial document showing an almost 20-year history of 13 significant semiconductor companies that, between 1995 and 2013, exited the DRAM market).

Mr. Daly will testify that, during the relevant period of 2015 to 2018, the Big Three DRAM IDMs spent more than one billion dollars and required roughly two years to develop a new DRAM technology process node, even though they were able to build on and leverage a foundation of the technology in several generations of prior process nodes. *See, e.g.*, Harald Bauer, Stefan Burghardt, Sid Tandon, and Florian Thalmayr, McKinsey & Co., Inc., "Memory: Are challenges ahead?," at 5 & Exh. 4 (Mar. 2016) (the cost of developing a leading-edge node (~20nm in 2014) was on the order of \$1 billion and the cost of a leading-edge factory to manufacture the product was about \$10 billion), <https://www.mckinsey.com/industries/semiconductors/our-insights/memory-are-challenges-ahead#>;

(BRACKETED MATERIAL CONFIDENTIAL – SUBJECT TO PROTECTIVE ORDER) Mr. Daly will testify that, of the Big Three DRAM IDMs, only Micron is close to a pure-play memory-chip manufacturer with publicly reported data, and during the relevant period roughly two-thirds of Micron's revenue came from DRAM. Samsung and SK Hynix, as conglomerates with many different businesses, do not publicly report DRAM-specific R&D expenditures. Micron annual reports on Form 10-K from 2013-2018 – the years of 25nm DRAM and Project M – reveal annual R&D expenditures ranging from \$931 million (2013) to \$2.141 billion (2018). [REDACTED]

(BRACKETED MATERIAL CONFIDENTIAL – SUBJECT TO PROTECTIVE ORDER) [REDACTED]

Because a logic foundry like UMC does not have DRAM technology for the immediately preceding process nodes, and thus cannot build on a current DRAM technology foundation, Mr. Daly will

testify that UMC would have required resources in money, engineers, and time substantially more than those expended by the Big Three DRAM IDM's to develop stand-alone DRAM products. While foundries such as UMC and GLOBAL FOUNDRIES would have prior generations of logic technology to leverage in attempting to develop DRAM, a logic foundries' technology, device structures, process recipes, and manufacturing know-how are not as directly applicable as those of DRAM IDM's.

Mr. Daly will testify that, directionally, the investments by DRAM IDM's to develop a process node suggest that a foundry would need to invest well into the nine figures over a period of years to develop stand-alone DRAM products and extend the technology roadmap, even if that DRAM is not the latest process node. That reasoning is consistent not only with the McKinsey analysis and Micron R&D expenditures, but also with his experience at GLOBALFOUNDRIES and industry knowledge. By comparison, the headline R&D expenditures committed by UMC and JHICC to Project M—notably, \$400 million over a five-year period, less than \$100 million per year—can barely be considered a down-payment on those required to develop the F32 / 25nm process node independently and from scratch. *See, e.g.,* USD-0353878, USD-0353878-HT-00001 (translation), & UMCDOJ-03102738 (Technology Cooperation Agreement between UMC and JHICC submitted to Investment Review Committee of Ministry of Economic Affairs of Taiwan on Mar. 11, 2016 and signed by the parties on May 13, 2016) (\$200 million JHICC payment to UMC per technology node plus \$300 million in R&D tools); *see also, e.g.,* UMCDOJ-00929234; UMCDOJ-00064380 (Stephen Chen PowerPoint presentation on “independent” “from scratch” technology development). (For comparison, UMC annual reports on Form 20-F with the U.S. Securities and Exchange Commission show that, in support of its core logic foundry business, UMC invested R&D at an average rate of \$421 million per year over the period 2013-2018 (lowest \$371.3 million in 2015; highest \$461.2 million in 2017).)

Mr. Daly will testify that he would have expected to see substantial documentation and discussion of Project M by the UMC Board of Directors and among the UMC senior leadership team, for several reasons:

- UMC is a public company whose shares are traded on the Taiwan and New York stock exchanges and which is therefore subject to securities laws;
- Project M was a material departure from UMC's core business;
- Project M expanded UMC's strategic position and exposure on mainland China;
- Project M presented competitive and business challenges, which challenges were especially daunting for UMC, because the DRAM technology was supposed to be developed independently and from-scratch, and UMC had no stand-alone DRAM product or foundry offering in their portfolio; further, even in its core logic foundry business, UMC was not and still is not a technology leader and is instead a “fast follower,” typically bringing technologies to market two to three years after market leader, TSMC (UMC's core logic foundry value proposition has been to be “TSMC-compatible”).

Among the documentation and discussion from UMC's Board and senior leadership team, Mr. Daly will testify that he expected to see:

- a clear statement of strategic objectives of the new business with supporting analysis of the market, competitive landscape, key success factors (KSFs), and UMC market positioning;

- thorough investment analyses and business plans;
- the explicit intended source of the DRAM process technology and memory product designs, be it joint development, licensing, or independent, from-scratch development effort;
- a detailed Technology Development Plan (*e.g.*, Product Requirements Document, reference UMC process technology, gap analysis between UMC reference process and target DRAM process (licensed or developed internally), the PDK-equivalent for DRAM product design, schedule/ timeline with test chips, cycles, and shuttles, Stage Gates with exit criteria, and Design of Experiments plan);
- a Resources Plan (*e.g.*, detailed operating budget, headcount, recruiting, manpower curve, and R&D capacity and facility resources);
- New tool acquisition anticipated (total capital expenditure plan), and fit with UMC R&D labs and efforts;
- Risk and Mitigation Plan (*e.g.*, market, technology, schedule, business, and political); and
- Program Governance (*e.g.*, progress reviews within UMC BOD and JHICC, likely with formal BOD decision on the proposal, with follow-ups and/or limits on execution performance that would trigger interim reviews with the BOD (technical, schedule, cost, etc.).

Mr. Daly will testify that he understands that the foregoing documents and information were requested from UMC in the request that appears in Exhibit 2.

Mr. Daly reviewed the documents and information produced by UMC in response to the Exhibit 2 request and other UMC document requests and did not find documentation indicating either UMC Board of Directors or UMC senior leadership team discussion he expected covering the approval, launch, planning, governance, control, and reporting of an independent, from-scratch DRAM development effort by a publicly traded foundry such as UMC.

Principal Opinion 3: Project M Resources Are Consistent with Technology Transfer, Not Technology Development

Mr. Daly will testify that, although the resources committed by UMC and JHICC to Project M are not sufficient for an independent, from-scratch development of DRAM technology by a logic foundry, they are roughly comparable in his experience with a transfer of technology from a third party. At GLOBALFOUNDRIES, Mr. Daly helped negotiate a strategic alliance on advanced technology with Samsung and the transfer of Samsung's 14 nm logic process technology to GLOBALFOUNDRIES. Mr. Daly also managed the initial post-acquisition integration of IBM's microelectronics business and the subsequent rationalization of the integrated R&D functions. Mr. Daly will compare those experiences at GLOBALFOUNDRIES with Project M.

Samsung

Mr. Daly will testify that he was responsible for negotiating GLOBALFOUNDRIES' licensing of 14 nm logic process technology from Samsung and for leading the transfer of that technology from Samsung's fab in South Korea to GLOBALFOUNDRIES' leading-edge fab in Malta, New York. At the time,

GLOBALFOUNDRIES and Samsung participated with IBM in a joint development agreement alliance for 14 nm logic process technology. The three companies participated in joint research and early development of the 14 nm logic technology, after which each company continued development work on its own. Samsung was outpacing GLOBALFOUNDRIES, so GLOBALFOUNDRIES decided to license the Samsung 14 nm implementation and discontinue GLOBALFOUNDRIES' own development work. Despite having come from a common foundation, the license value paid by GLOBALFOUNDRIES to Samsung was multiple hundreds of millions of dollars in payments and royalties. The technology transfer was an extraordinarily complex and detailed process, including:

- Transfer of information on process flows, recipes, equipment configurations, mask sets, metrology measurements, and the transfer of physical wafers for matching purposes. Samsung and GLOBALFOUNDRIES exchanged more than 5,000 files and more than 500,000 tool, material, and process specifications in order to match them (the objective was to achieve "copy exact");
- Development of a detailed "delta analysis" (gap analysis), comparing the GLOBALFOUNDRIES' existing 14 nm process flow, tool set, materials, used and facilities infrastructure, on the one hand, with that of Samsung, on the other hand, to identify gaps and required new investments;
- Investments in new tooling to assure GLOBALFOUNDRIES' capability to meet parametric performance of Samsung, including the introduction of more than 50 new raw materials; and
- Installation and qualification of new tooling and materials, followed by several waves of wafer processing the test vehicles to qualify the Samsung process in New York.

The planned duration of the 14 nm logic technology transfer from contract signing to customer qualification of product shipments was approximately six quarters. GLOBALFOUNDRIES staffed a discrete organization of program management and process integration engineering, supported by dedicated module/equipment engineers, totaling more than 100 engineers within the first 90 days. This technology transfer "receiver" group was supplemented by 10-20 Samsung "sending" engineers, which number fluctuated over the course of the transfer. "Home" and "Away" teams were established by both companies to provide in-person, on-site, dedicated transfer of know-how to accompany the documentation.

(BRACKETED MATERIAL CONFIDENTIAL – SUBJECT TO PROTECTIVE ORDER) Mr. Daly will testify that the level of process integration and module/equipment engineering resources committed by GLOBALFOUNDRIES for the Samsung technology transfer and engineering support of the initial 14 nm logic program were roughly in line with second-half 2016 levels found in UMC manpower plans, with a subsequent ramp to UMC's 2018 planned levels as process extensions and additional products were added. *See, e.g., USD-0844715.* Key differences in this comparison are: (1) GLOBALFOUNDRIES staffed to those initial levels in roughly one quarter, while UMC did not do so for two to three quarters; and (2) the GLOBALFOUNDRIES resources were in explicit support of a technology transfer, while UMC has represented that they were pursuing an independent, from-scratch R&D effort, which would require a significantly larger resources investment. [REDACTED]

The Samsung and Micron experiences reinforce that UMC resource allocation was in line with a technology transfer – or in UMC’s case, technology absorption – which is consistent with Stephen Chen’s experience absorbing Elpida (Micron) technology at Rexchip (MMT).

IBM

Mr. Daly will testify that he led GLOBALFOUNDRIES’ initial post-acquisition integration of IBM’s microelectronics unit and subsequent rationalization of the combined R&D resources in support of 10 nm and 7nm logic process technology development programs. GLOBALFOUNDRIES’ primary motivations for acquiring the IBM unit were to gain technology, technologists, and patents. For decades, IBM was a leader in semiconductor R&D and was the center of a logic joint development partnership with Samsung and GLOBALFOUNDRIES. Acquisition of an experienced R&D team was necessary for GLOBALFOUNDRIES to be able to attempt to compete for leading-edge logic foundry work. Mr. Daly will testify that the combined IBM-GLOBALFOUNDRIES R&D program on the 10 nm and 7 nm logic process technologies demonstrate the differences between an organic, independent, stand-alone R&D initiative, on the one hand, and technology transfer, on the other hand. Mr. Daly will testify that the key differences include:

- R&D starts with an unknown solution to a desired technical specification(s); technology transfer starts with a known solution to typically a mature, high yielding process technology;
- R&D is a process of innovation, discovery, and ideation; technology transfer is a process of a highly disciplined transfer of existing knowledge;
- R&D involves dealing with new technologies, materials, and tools; technology transfer attempts to implement as close to a “copy exact” process as possible with the objective of minimizing differences and variation between the sending and receiving fabs;
- R&D is about experimentation (a key technique is the DoE or design of experiment), exploring limits of technology and optimization, using iterations, short-loops and parallel runs to speed the process; technology transfer is about replication of a known, detailed technical solution developed by another party;
- R&D must include the development of the design tools (PDK) in parallel with the development of the process technology; technology transfer may include minor changes to an existing set of design tools as necessitated by minor variations in the process technology implementation between the sending and receiving fabs;
- The size of the R&D team for a leading-edge logic semiconductor process technology is in the range of 700-1,000 engineers; the size of a team to transfer a technology and mature its implementation (e.g., cost, yield, quality) in a fab is between 100-200 engineers; and
- A new node R&D effort typically takes about two years; a technology transfer typically takes 9-15 months, depending on several factors. Those factors include the relationship history between the parties (e.g., same company, same IT systems, language), the complexity of the product, whether there has been a prior transfer, and the extent of new tools, materials, and facilities infrastructure required. The time to buy, install, and qualify those items can

add months to a technology transfer.

Based on his experience and by reviewing documents in the case, Mr. Daly will testify that the level of Project M resources is consistent with a technology transfer. Mr. Daly will explain that UMC business records show that Stephen Chen planned to enter the stand-alone DRAM industry before his first day on the job at UMC; that Stephen Chen knew he needed both a DRAM product design and a DRAM process to succeed and that Chen worked with UMC leadership in support of that plan. *See, e.g.*, UMCDOJ-00158460; UMCDOJ-03127189; UMCDOJ-00157908.

Mr. Daly may further testify that his review of the documents in the case suggests that Stephen Chen's timeline and resources for Project M were aggressive. For example, (1) Stephen Chen immediately solicited DRAM product designs from Ultra Memory, Inc. (UMI), even prior to developing the DRAM technology. Mr. Daly will explain that this is significant because UMI was a design house, and the early solicitation of UMI, prior to UMC's development of DRAM, suggests that Stephen Chen had already decided to develop DRAM; and (2) by March 2016, Stephen Chen was already focused on ordering the tools to make DRAM. *See e.g.*, UMCDOJ-01201226. Mr. Daly will suggest that this means that Project M would already have had to have developed the process and design parameters sufficiently to be ordering the tool to manufacture and produce DRAM. Mr. Daly will also note that UMI was Micron's design house. Mr. Daly will offer the opinion that timeframe is not consistent with new technology development.

Further, Mr. Daly may testify that he reviewed documents that showed heavy reliance by Project M on former Micron employees, and use of Micron nomenclature, and offer that the timelines for Project M reflect the ability to accomplish aggressive timelines because of the use of Micron's information, employees with knowledge, and contracting with UMI. *See e.g.*, UMCDOJ-03127189, UMCDOJ-00158460, UMCDOJ-00158789, & UMCDOJ-00929231.

Principal Opinion 4: Project M injured Micron

Mr. Daly will testify that Project M injured Micron in two ways. *First*, Mr. Daly will testify that the exfiltration of Micron's trade secrets removed Micron's control over its trade secrets. Intellectual property, which includes, trade secrets and other confidential information, are the lifeblood of technology firms, especially in the semiconductor industry. Unlike a patent, trade secrets are valuable only if they are secret. The existence of Micron's trade secrets in the wild is itself injury. UMC's technology transfer documentation illustrates the breadth of the DRAM technology transferred from UMC to JHICC. *See* UMCDOJ-06920276 (TOC for September 2018 TT package); UMCDOJ-06920283 (demonstrating UMC employee sign-off validating support for each component of the transfer).

Second, Mr. Daly will testify that if JHICC had manufactured DRAM, Micron and other Big Three DRAM IDMs, Samsung and SK Hynix, would have lost market share, sales, revenue, and profits. The economic damage would likely have been severe. Presentations and statements by Stephen Chen reveal a technology roadmap to achieve near technological parity with and the technical and financial wherewithal to compete against Micron and the other Big Three DRAM IDMs by 2020. *See, e.g.*, UMCDOJ-00159863 (Stephen Chen e-mail message to T R Yew dated Jan. 27, 2016 stating "[t]arget is to . . . drive to 18nm node in 4 years"); UMCDOJ-00159864 (PowerPoint slides attached to Stephen Chen e-mail message entitled "Project M Overall Schedule Review" noting on slide 4 that "Project M will get behind competitor [sic – competitors are listed as Samsung, Micron, and SK Hynix] about 0.5~1

generation at 2020"). That objective is well beyond the establishment of an indigenous Chinese DRAM firm to address local needs, supply specialty DRAM, or fill niche markets.

(BRACKETED MATERIAL CONFIDENTIAL – SUBJECT TO PROTECTIVE ORDER) Mr. Daly will testify that JHICC would have been a mega fab. JHICC publicly presented a strategy to construct two 300mm DAM fabs with a capacity of 240,000 wafer outs per month or approximately 2.88 million wafers per year. See D-0000104. Many factors determine the revenue value of that level of output, including product competitiveness, yield, DRAM pricing in line with industry supply-demand dynamics, and success in customer qualification of JHICC parts. Many scenarios could be developed based on the effective output of JHICC and the pricing/revenue value of wafers produced. Conservatively assuming two million wafer outs annually at \$3,000 to \$4,000 per wafer value, JHICC would have generated annual revenue of \$6 million to \$8 million. For perspective, Mr. Daly will explain that JHICC's business alone would have been larger than Micron's entire PRC sales and would necessarily have severely undercut the market position, financial performance, and shareholder value of the top three DRAM IDMs, especially Micron. Micron has about 20% global DRAM share (see, e.g., Micron 2020 annual report on Form 10-K and Business Quant "DRAM's Market Share by Company (Q1 2014 – Q4 2021)", <http://businessquant.com/dram-market-share-by-company>) and [REDACTED]

[REDACTED] Roughly 20% of Micron's annual revenue is shipped to China-headquartered companies. See Micron annual reports on Form 10-K. Micron's exposure to a successful UMC/JHICC strategy could have been disproportionate to the exposure of Samsung and SK Hynix. If trade secret misappropriation is established, Micron would effectively have been competing against its own technology when competing for customer DRAM sockets against JHICC. What is more, Micron (and Samsung and SK Hynix) would have been exposed to lost market share, sales, and profits not only in the PRC, but outside the PRC as well, because JHICC was positioning to compete in the global DRAM market. In support of his opinion, Mr. Daly also considered, among other documents:

- Micron 2020 annual report on Form 10-K (Micron memory product shipments to customer companies with headquarters in mainland China and Hong Kong totaled \$5.209 billion and \$4.129 billion in 2019 and 2020 respectively);
- USD-0844602 ("Prospect of China Semiconductor Industry and Fujian Semiconductor": joint development by UMC and JHICC showing PRC's importance as a semiconductor market; that UMC and JHICC intend to help China achieve the goal of 40% chip self-sufficiency by 2025, and that China semiconductor will certainly spring up," reinforcing an intent for UMC/JHICC to be part of the larger China strategy to both displace Micron (and Samsung and SK Hynix) share in China, and to strategically position for global share influence over time).
- IC Insights Research Bulletin, May 20, 2021, "Memory Upswing Returns, New Record High Expected in 2022." This industry document forecasts an increase in the size of the memory market to \$155.2B in 2021, 56% (or \$86.912B) of which is DRAM. If Micron were to retain its market share position of ~22.5% into 2021, and China-headquartered customers remain at ~20% of its revenue, the forecast revenue at risk for Micron due to the loss of access to, or displacement from, China's DRAM market, would be on the order of \$3.911B.

Principal Opinion 5: Project M Benefited JHICC and the People's Republic of China

Mr. Daly will testify that Project M helped the PRC advance its four-decade-old strategic goal of establishing a domestic semiconductor industry, by creating an industry competitive DRAM IDM. Project M would further the PRC's reputation in showing that China was no longer simply an assembler of other countries' technology, which China's electronics assembly contract manufacturing industry represents. Project M would have provided a controllable strategic domestic supply of DRAM products. Beyond the tactical benefit of a domestic source of memory chips for commercial applications, Project M would also provide a secure, domestic source of supply for China's military applications. Indeed, Project M documentation shows that supporting the military with DRAM chips from JHICC was intended, despite public representations to the contrary.

Mr. Daly will testify that, over a period of four decades, the PRC has tried to develop an indigenous semiconductor manufacturing industry to reduce its dependence on the global supply chain, reduce chip imports, capture more of the value chain and the associated revenue and profit, and increase jobs and technical skills in mainland China. The PRC has allocated and spent billions of dollars on this strategy, including the identification and funding of national champion firms in the semiconductor manufacturing segment, and it has encouraged Chinese provinces and municipalities to join the national funding effort. This motive has become even stronger today in response to U.S. trade sanctions, as the PRC redefined its objective to one of becoming self-sufficient in semiconductor production. JHICC represents a textbook example of a firm funded by Chinese government entities (both national and regional) with attendant oversight and control by those entities. In support of his opinion, Mr. Daly considered, among other documents:

- USD-0000308: A Semiconductor Industry Association confidential assessment of China's semiconductor initiatives across 12 cities, including Jinjiang, Fujian Province.
 - Pages 7-12 summarize the rationale, investment levels, funding mechanisms, and broad strategy for the region, and how JHICC fits; and
 - Page 8: "Officials stated Jinjiang has attained national recognition for its IC industry by both the central government and the National IC Fund, with the Jinhua IC project being granted 'national strategy' status."
- UMCDOJ-00120703: written testimony by Mr. Jimmy Goodrich of the Semiconductor Industry Association (**SIA**) to the U.S-China Economic and Security Review Commission (Apr. 26, 2016), summarizing China's recently published 13th Five-Year Plan. Notably, on page 2, "the Chinese Government is implementing policies to develop a robust semiconductor capability with the goal of establishing a leadership position in all major segments of the semiconductor industry by 2030."
- USD-0000268: an SIA confidential assessment and member update on the memory industry, with a focus on China's goals, subsidies, and domestic fab investments. Pages 21-24 highlight China's efforts to gain access to memory technologies.
- "Learning the Superior Techniques of the Barbarians – China's Pursuit of Semiconductor Independence," by James A. Lewis, Center for Strategic and International Studies, January 2019. Particularly relevant portions considered by Mr. Daly include:

- Page 22 regarding China's security motivations and targeting of memory chips as the primary initial target for M&A and investments, in hopes of it leading to an upward path to the most sophisticated semiconductors
- Page 26 regarding the tight linkage of national security and the semiconductor industry, and
- Page 8 regarding the risk of and potential for market distortion from China's government subsidization in chip manufacturing. "China's government-subsidized expansion will squeeze semiconductor firms in other countries, shrinking their income and numbers and reducing the ability of semiconductor producers to invest in R&D. The overall effect of China's investments will be to weaken the global industry and slow the pace of semiconductor innovation."
- "A new world under construction: China and semiconductors" by Christopher Thomas, McKinsey & Co., Inc., Nov. 1, 2015.
- USD-0844602 "Prospect of China Semiconductor Industry and Fujian Semiconductor"
- UMCDOJ-00161265 & UMCDOJ-00161264. UMC Interview Q&A Primer, March 15, 2016, prepared by Stephen Chen, Travis Cho, and Sandy Kuo, in preparation for review with Chairman Stan Hung. "China market is not truly a free market. Jinhua [Chinese characters omitted], being a government-sponsored company, will be able to sell in areas that are not reachable by non-governmental sponsored companies." Among the applications cited are military specs.

Mr. Daly also considered Dieter Ernst, "From Catching Up to Forging Ahead? China's Prospects in Semiconductors," East-West Center (2015); Kevin Meehan, Florian Hoppe, Jihyo Lee & Steven Lu, "China Chases Chip Leadership," Bain & Company (2016); US-China Business Council, "China's Strategic Emerging Industries: Policy, Implementation, Challenges & Recommendations" (Mar.2013); Antonio Varas, Raj Varadarajan, Jimmy Goodrich & Falan Yinug, BCG and SIA, "Government Incentives and US Competitiveness in Semiconductor Manufacturing" (Sept. 2020); PricewaterhouseCoopers LLP, "China's impact on the semiconductor industry: 2016 update" (Jan. 2017); Will Hunt, Saif M. Khan & Dahlia Peterson, Center for Security and Emerging Technology, "China's Progress in Semiconductor Manufacturing Equipment Accelerants and Policy implications" (Mar. 2021).

Mr. Daly will testify that Project M had great potential to establish a domestic PRC DRAM industry because UMC and JHICC acquired the DRAM technology jointly and JHICC thus learned critical knowhow and skills. JHICC and UMC operated as a contractual joint venture with integrated operations in the acquisition and alteration of DRAM technology. Examples of joint venture activities considered by Mr. Daly include:

- JHICC and UMC entered into a multi-year, two technology node technology cooperation agreement (the **TCA**) with resulting IP rights to be held jointly. See USD-0353878 HT-0001.
- On May 27, 2016, JHICC and UMC contracted for chip design services with UMI jointly with the design services agreement referencing the TCA and with resulting IP rights to be held jointly. See TAIWANHD-02165472 & TAIWANHD-02165473.

- JHICC and UMC recruited jointly, including a key Santa Clara, California on October 23, 2016. *See* D-0000120, D-0000053, D-0000054, D-00000057, D-00000093, D-00000094, D-00000098, D-00000104, USD-0846450, USD-0846451.
- JHICC and UMC engaged with SEMs jointly. *See* USD-0348331, USD-0663510, USD-0663511, USD-0663512.
- JHICC and UMC compensated and incentivized employees jointly (Project M employee bonuses were payable by JHICC and only on the mainland using a mainland bank). *See* UMCDOJ-06920288.
- JHICC and UMC exchanged staff jointly, with several UMC employees going to work for JHICC. (Project M employed many engineers from MMT, who had joined UMC over the course of Project M. Many Project M engineers subsequently went to work at JHICC. *See* UMCDOJ-06920275.)
- Stephen Chen served as an officer of JHICC and UMC jointly (UMC's Board of Directors waived UMC's policy prohibiting joint employment). *See* UMCDOJ-06920225.
- JHICC and UMC coordinated management presentation and updates to China stakeholders in JHICC jointly. *See* USD-0854382.
- JHICC and UMC filed patents covering the DRAM technology and products jointly. *See* USD-0844776, pages 35-38.

Bases and Reasons for Expert Testimony

The bases and reasons for Mr. Daly's testimony are his engineering education and training, industry knowledge and experience, discussions with industry participants, and review of documents.

The government hereby reserves the right to supplement this Notice as warranted. Pursuant to Criminal Rule 16(b)(1)(C), the Government requests that the defendant disclose any testimony that it intends to use under Rules 702, 703, and/or 705 of the Federal Rules of Evidence as evidence at trial.

Exhibit 1: Additional Documents Considered by Terrence Daly

BEGDOC	FILENAME
D-0000001	
D-0000001_HT-00001	
D-0000003	
D-0000008	
D-0000010	
D-0000048	
D-0000049	
D-0000053	
D-0000054	
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D-0000098	
D-0000104	
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D-0000254	
D-0000254_HT-00001	
D-0000266	
D-0000266_HT-00001	
D-0000434_HT-00001	
D-0000682_HT-00001	
D-0000690_HT-00001	
D-0000714_HT-00001	
D-0001012	
D-0001012_HT-00001	0000034.eml
D-0001327	Rexchip - Elpida Process Update 20100730.ppt
TAIWANHD-00004651	25nm_4GLP3_下地IDR資料_1.pdf
TAIWANHD-00011576	Micron Fab16 New Technology Transfer by Elp History.ppt
TAIWANHD-00017400	Overview of the methodology for transfer by Elp.ppt
TAIWANHD-00032486	Technology Transfer Introduction 20121115.ppt
TAIWANHD-00032488	Micron Fab16 New Technology Transfer by Elp History.ppt
TAIWANHD-00032489	Overview of the methodology for transfer by Elp.ppt
TAIWANHD-00032490	Technology Transfer Introduction 20121115.ppt
TAIWANHD-00032492	Technology Transfer Introduction 20121115.ppt
TAIWANHD-00032493	Overview of the methodology for transfer by Elp.ppt
TAIWANHD-01841534	Overview of the methodology for transfer by Elp.ppt
TAIWANHD-01841561	Overview of the methodology for transfer by Elp.ppt

Exhibit 1-2

TAIWANHD-01844584	Micron Fab16 New Technology Transfer by Elp History.ppt
TAIWANHD-01844585	Overview of the methodology for transfer by Elp.ppt
TAIWANHD-01844589	Overview of the methodology for transfer by Elp.ppt
TAIWANHD-01847316	Overview of the methodology for transfer by Elp.ppt
TAIWANHD-01847349	Technology Transfer Introduction 20121115.ppt
TAIWANHD-01847351	Micron Fab16 New Technology Transfer by Elp History.ppt
TAIWANHD-01847372	Micron Fab16 New Technology Transfer by Elp History.ppt
TAIWANHD-01847534	Overview of the methodology for transfer by Elp.ppt
TAIWANHD-02121050	Overview of the methodology for transfer by Elp.ppt
TAIWANHD-02145180	Micron Fab16 New Technology Transfer by Elp History.ppt
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TAIWANHD-02160089	Meeting minute 20151207 3.xlsx
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TAIWANHD-02165470	0000118.eml
TAIWANHD-02165471	F32nm DSA UMI and UMC signed.pdf
TAIWANHD-02165472	F32nm DSA UMI and UMC signed.pdf
TAIWANHD-02165473	020a-Design ServiceAgreement_20161107.docx
TAIWANHD-02165474	Design agreement exhibit A.pdf
TAIWANHD-02165500	020a-Design ServiceAgreement_20161107.docx
TAIWANHD-02165501	Design agreement exhibit A.pdf
TAIWANHD-02165502	0000149.eml
TAIWANHD-02165503	Ultramemory Profile 20161102.pptx
TAIWANHD-02165515	Ultramemory Profile 20161102.pptx
TAIWANHD-02165516	Ho Testimony Final
TAIWANHD-02165518	Answer to Criminal Complaint No. 14 (Witness Jian-Ting Ho) 04.17.2020
UMC-T-00000009	Taiwan Taichung Municipal Court Criminal Judgment (main text)
UMC-T-00000225	
UMC-T-00000318	PM1_2018 方針展開_工作表 v1 (version 1).xlsb
UMCD-0000046	DRAM Development Progress Report_Sep_2017簡_0904.pptx
UMCDOJ-00000074	
UMCDOJ-00009666	F32 Process Training Material 20170904.pptx
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UMCDOJ-00009720	BM Pitch discussion.xlsx

Exhibit 1-3

UMCDOJ-00010229	DRAM Development for NCKU talk v2_20161201.pptx
UMCDOJ-00010269	DRAM PM1研發進度 UMC_201805_簡_v4.pptx
UMCDOJ-00010355	F32&F32s development status update-20171228(繁).pptx
UMCDOJ-00010378	M project introduction for Toshiba 0323.pptx
UMCDOJ-00010466	M project introduction_0330.pptx
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UMCDOJ-00010612	Strategy template Stephen_0722.pptx
UMCDOJ-00010671	Tool Demo Plan_07202016.pptx
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UMCDOJ-00063848	1949.Ind
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UMCDOJ-00063988	P 81 of PM1 Annual report for JHICC_Dec_2016_v2.pptx
UMCDOJ-00063991	008.Ind
UMCDOJ-00064094	Wonik IPS Products in DRAM Production-2015-1203.pdf
UMCDOJ-00064128	012.Ind
UMCDOJ-00064130	F32 6F2(3x2,2x3) discussion-JT_20160111_rev1.pptx
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UMCDOJ-00064150	TechInsights-DRAMRoadmap2014.ppt
UMCDOJ-00064156	1.xls
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UMCDOJ-00064179	Project M Milestone V2_20160118-neillee.pptx
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UMCDOJ-00064224	059.Ind
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UMCDOJ-00064227	Risk assessmemt.pptx

Exhibit 1-4

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Exhibit 1-5

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UMCDOJ-00116086	2017-0721-UMC-DRAM-OTP-Proposal(Spec-schedule)(V1).pptx
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UMCDOJ-00116089	doc15168420170601170101.pdf
UMCDOJ-00117163	3767.msg
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UMCDOJ-00119383	3860.msg

Exhibit 1-6

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UMCDOJ-00120078	4177.msg
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UMCDOJ-00120218	4189.msg
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UMCDOJ-00120234	4335.msg
UMCDOJ-00120235	DRAM Development for NCKU talk v1.pptx
UMCDOJ-00120684	SIA China 13 5-year plan.pdf
UMCDOJ-00120685	4486.msg
UMCDOJ-00120723	AGS_Executive_Overview_UMC (25 Oct'16).pdf
UMCDOJ-00121172	4534.msg
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UMCDOJ-00121191	4923.msg
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UMCDOJ-00123046	5545.msg

Exhibit 1-7

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Exhibit 1-8

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Exhibit 1-9

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Exhibit 1-10

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Exhibit 1-11

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Exhibit 1-12

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Exhibit 1-13

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Exhibit 1-14

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Exhibit 1-15

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Exhibit 1-16

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Exhibit 1-17

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Exhibit 1-18

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Exhibit 1-19

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Exhibit 1-20

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Exhibit 1-21

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Exhibit 1-22

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Exhibit 1-23

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UMCDOJ-00159913	Manpower estimation for Project M_20160216.pptx
UMCDOJ-00160103	Manpower estimation for Project M_20160216.pptx
UMCDOJ-00160126	0947.Ind
UMCDOJ-00160130	DR合作案Q&A_20160214.docx
UMCDOJ-00160131	Manpower estimation for Project M_20160216.pptx
UMCDOJ-00160132	1001.Ind
UMCDOJ-00160148	福建晋华集成电路 存储器生产线项目申请报告(草稿) 0225V2.doc
UMCDOJ-00160228	1.xls
UMCDOJ-00160230	1120.Ind

Exhibit 1-24

UMCDOJ-00160356	1139.Ind
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UMCDOJ-00161022	1167.Ind
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UMCDOJ-00161236	1173.Ind
UMCDOJ-00161238	1172.Ind
UMCDOJ-00161260	New Business organization & manpower_201603.xlsx
UMCDOJ-00161261	1175.Ind
UMCDOJ-00161263	Interview Q&A_201603.pptx
UMCDOJ-00161264	1183.Ind
UMCDOJ-00161265	1194.Ind
UMCDOJ-00161283	New Business organization & manpower_201603.xlsx
UMCDOJ-00161554	PM weekly_20160317.pptx
UMCDOJ-00161555	1197.Ind
UMCDOJ-00161556	Stephen Chen.pptx
UMCDOJ-00161574	1205.Ind
UMCDOJ-00161575	1206.Ind
UMCDOJ-00161592	DRAM S,H,M SA SWD 160317.pptx
UMCDOJ-00161595	1224.Ind
UMCDOJ-00161597	SN Module_ver2.doc
UMCDOJ-00161612	SC Module_ver2.doc
UMCDOJ-00161616	SOD Module_ver2.doc
UMCDOJ-00161617	Wet Module_ver2.doc
UMCDOJ-00161618	BL Module_ver2.doc
UMCDOJ-00161619	Etch Module_ver2.doc
UMCDOJ-00161621	1247.Ind
UMCDOJ-00161623	Interview Q&A- phase 1 V4.0.pptx
UMCDOJ-00161657	1341.Ind
UMCDOJ-00161661	1401.Ind
UMCDOJ-00162086	1403.Ind
UMCDOJ-00162378	1409.Ind
UMCDOJ-00162384	0261.Ind
UMCDOJ-00162410	3690.Ind
UMCDOJ-00162476	Project-M Progress Report_May 2017.pptx
UMCDOJ-00163339	4679.Ind
UMCDOJ-00163340	1442.Ind
UMCDOJ-00164810	NBD manpower update_04082016.pptx
UMCDOJ-00168276	PROJECT-M-7_HR plan.pptx
UMCDOJ-00168279	1608.Ind
UMCDOJ-00168285	20160418_UMC_Fujian_Structure_Interest CF.pdf
UMCDOJ-00168507	Project M EQ Procurement Strategy & Achievement.pptx

Exhibit 1-25

UMCDOJ-00168508	Project M EQ Procurement Strategy & Achievement.pptx
UMCDOJ-00170038	Project M EQ Procurement Strategy & Achievement.pptx
UMCDOJ-00170166	3330.Ind
UMCDOJ-00170186	M Team.pdf
UMCDOJ-00173438	3385.Ind
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UMCDOJ-00173551	3784.Ind
UMCDOJ-00173557	picture1.gif
UMCDOJ-00174878	picture2.gif
UMCDOJ-00174888	5232.Ind
UMCDOJ-00174889	DRAM Development for NCKU talk v2_20161202.pptx
UMCDOJ-00178843	5623.Ind
UMCDOJ-00178844	动态随机存储器研发年度报告(2016.12)-1.pptx
UMCDOJ-00179936	1.xlsx
UMCDOJ-00179937	025.Ind
UMCDOJ-00179970	18.Ind
UMCDOJ-00186555	20.Ind
UMCDOJ-00186949	Reference_sf_20151224.xls
UMCDOJ-00186967	21.Ind
UMCDOJ-00186968	Information Security-Ryan-20151225.pptx
UMCDOJ-00186976	38.Ind
UMCDOJ-00186977	Reference_sf_20151230.xlsx
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UMCDOJ-00187045	Project M Milestone_20151228.pptx
UMCDOJ-00187046	UMI_華Pj Monthly Mtg_20170214.pdf
UMCDOJ-00187048	20180612 4Gb DDR3 Market Brief.pptx
UMCDOJ-00241796	PM1 Annual report for JHICC_Dec_2016_v3.pptx
UMCDOJ-00246407	107.Ind
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UMCDOJ-00366462	022.Ind
UMCDOJ-00366463	Litho process parameter table 2015 1214.xls
UMCDOJ-00366471	031.Ind
UMCDOJ-00366472	100.Ind
UMCDOJ-00366475	101.Ind

Exhibit 1-26

UMCDOJ-00366535	110.Ind
UMCDOJ-00366536	Key process development discussion-Project M-20151224.pptx
UMCDOJ-00366538	111.Ind
UMCDOJ-00366540	135.Ind
UMCDOJ-00366546	Milestone20151228.pptx
UMCDOJ-00366563	022.Ind
UMCDOJ-00366565	Project M next item follow up report after flow discussion -20160114.pptx
UMCDOJ-00366614	1.xlsx
UMCDOJ-00366616	025.Ind
UMCDOJ-00366620	6F2 cell options_Project M-20160114_SF update-rev2.pptx
UMCDOJ-00366628	091.Ind
UMCDOJ-00366630	096.Ind
UMCDOJ-00366739	105.Ind
UMCDOJ-00366742	145.Ind
UMCDOJ-00366744	068.Ind
UMCDOJ-00366757	277.Ind
UMCDOJ-00366835	DPT comparison.pptx
UMCDOJ-00368383	0776.Ind
UMCDOJ-00368386	picture1.gif
UMCDOJ-00411064	217.Ind
UMCDOJ-00411065	華_Design_Study_20160111.pptx
UMCDOJ-00414602	Project-M Progress Report_201712_v2.pptx
UMCDOJ-00414603	Project M master plan_v1.xlsx
UMCDOJ-00443520	華_Design_Study_20160203.pptx
UMCDOJ-00488766	華_Design_Study_鄒世芳-20160111.pptx
UMCDOJ-00488911	Project M_Module Weekly Report_20160316_sf tzou.pptx
UMCDOJ-00489264	1.xls
UMCDOJ-00489665	01.Ind
UMCDOJ-00489682	25nm RG HM ETCH Half Etch Issue Summary-1.ppt
UMCDOJ-00493109	N2 WLT on S-DRM.pptx
UMCDOJ-00493110	S-DRM DRM Process BKM.pdf
UMCDOJ-00493123	03.Ind
UMCDOJ-00493124	16.Ind
UMCDOJ-00493157	Project M Milestone_20151228.pptx
UMCDOJ-00493457	Project M_Module Weekly Report_20160323_sf tzou.pptx
UMCDOJ-00493607	Project M master plan_v1.xlsx
UMCDOJ-00493698	110.Ind
UMCDOJ-00680385	Key process development discussion-Project M-20151224.pptx
UMCDOJ-00838207	2284.Ind
UMCDOJ-00838209	动态随机存储器研发年度报告 (2016.12).pdf
UMCDOJ-00925075	3596.Ind

Exhibit 1-27

UMCDOJ-00925076	picture1.gif
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UMCDOJ-00927585	Presentation 20170209 BoD_rev3.pptx
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UMCDOJ-00927604	picture1.gif
UMCDOJ-00928488	TechInsights-DRAMRoadmap2014.ppt
UMCDOJ-00928490	18.Ind
UMCDOJ-00928547	Mask layer_minimum pitch.xlsx
UMCDOJ-00929106	Layer_mapping_example.xlsx
UMCDOJ-00929107	picture1.gif
UMCDOJ-00929108	27.Ind
UMCDOJ-00929109	TechInsights-DRAMRoadmap2014.ppt
UMCDOJ-00929153	1.xls
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UMCDOJ-00929208	44.Ind
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UMCDOJ-00929217	picture2.gif
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UMCDOJ-00929230	Milestone20151228.pptx
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UMCDOJ-01114828	Manpower estimation for Project M_20160216.pptx
UMCDOJ-01134226	Manpower estimation for Project M_20160216.pptx
UMCDOJ-01134230	2529.Ind
UMCDOJ-01134256	UMI_meeting_032816.pdf
UMCDOJ-01136636	3425.Ind
UMCDOJ-01136637	1978.Ind
UMCDOJ-01140557	Ultramemory Profile.pptx
UMCDOJ-01146535	華_Design_Study_20160203.pptx
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UMCDOJ-01171407	2017.09.13 Ultramemory 文件分發記錄 from TDS.xlsx
UMCDOJ-01171445	華Pj F32.pdf
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UMCDOJ-01174004	UMI_meeting_041416.pdf

Exhibit 1-28

UMCDOJ-01196891	華_Design_Study_20160310.pdf
UMCDOJ-01196892	Manpower estimation for Project M_20160216.pptx
UMCDOJ-01196901	Manpower estimation for Project M_20160216.pptx
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UMCDOJ-01201047	25 beyond for S_20150913.ppt
UMCDOJ-01201226	Presentation 20150917 FJ B.pptx
UMCDOJ-02966031	RD Milestone \$\$.xlsx
UMCDOJ-02966542	019048.msg
UMCDOJ-02967175	019224.msg
UMCDOJ-03081278	DRAM Development for NCKU talk v2_20161202.pptx
UMCDOJ-03081850	1.xlsx
UMCDOJ-03081851	027945.msg
UMCDOJ-03081872	关于专用研发设备采购事宜的备忘录-拓维代拟稿.docx
UMCDOJ-03090074	037179.msg
UMCDOJ-03090075	037406.msg
UMCDOJ-03096816	More information for Jinhua.docx
UMCDOJ-03097401	047317.msg
	议案8：关于国家专项建设基金申报情况以及基金承接投放建议的报告（ 20160504书面稿）(1).doc
UMCDOJ-03097407	047340.msg
UMCDOJ-03102607	054152.msg
UMCDOJ-03102609	20160308晋华公司第一届第二次董事会会议纪要.docx
UMCDOJ-03106734	福建晋华集成电路 存储器生产线项目申请报告（草稿）0225V2.doc
UMCDOJ-03106735	071519.msg
UMCDOJ-03108565	075166.msg
UMCDOJ-03124928	075167.msg
UMCDOJ-03127189	Company profile.pdf
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UMCDOJ-03127192	076750.msg
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UMCDOJ-03129862	7698.Ind
UMCDOJ-03798635	0738.Ind
UMCDOJ-03798640	103.Ind
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UMCDOJ-04362042	Manpower estimation for Project M_20160216.pptx
UMCDOJ-04362161	Manpower estimation for Project M_20160216.pptx

Exhibit 1-29

UMCDOJ-04369600	3602.Ind
UMCDOJ-04369629	20170307 Memory Market (Specialty DRAM)c.pdf
UMCDOJ-04381484	0946.Ind
UMCDOJ-04381485	Manpower estimation for Project M_20160216.pptx
UMCDOJ-04396702	Manpower estimation for Project M_20160216.pptx
UMCDOJ-04396705	Manpower estimation for Project M_20160216.pptx
UMCDOJ-04396712	6142.Ind
UMCDOJ-06152599	Resume_py_2015.docx
UMCDOJ-06210713	Resume_py_2015.docx;x-apple-part-url
UMCDOJ-06210715	Manpower estimation for Project M_20160216.pptx
UMCDOJ-06210720	1041028_13-3會議紀錄_clean.pdf
UMCDOJ-06213080	1041028_13-3會議紀錄節錄本 (for GC).pdf
UMCDOJ-06920171	1041216_13-4會議紀錄_clean.pdf
UMCDOJ-06920177	1050316_13-5會議紀錄_clean.pdf
UMCDOJ-06920179	1050427_13-6會議紀錄_clean.pdf
UMCDOJ-06920184	1050511_13-7會議紀錄_clean.pdf
UMCDOJ-06920195	1050615_13-8會議紀錄_clean.pdf
UMCDOJ-06920199	1050727_13-9會議紀錄_clean.pdf
UMCDOJ-06920203	1051026_13-10會議紀錄_clean.pdf
UMCDOJ-06920208	1051214_13-11會議紀錄(無附件)_clean.pdf
UMCDOJ-06920213	1060222_13-12會議紀錄_clean.pdf
UMCDOJ-06920219	1060222會議紀錄節錄本(for GC).pdf
UMCDOJ-06920225	1060426_13-13會議紀錄_clean.pdf
UMCDOJ-06920237	1060614_13-14會議紀錄clean.pdf
UMCDOJ-06920239	1060726_13-15會議紀錄_clean.pdf
UMCDOJ-06920247	1061025_13-16會議紀錄_clean.pdf
UMCDOJ-06920252	1061213_13-17會議紀錄(節錄本for GC).pdf
UMCDOJ-06920260	1061213_13-17會議紀錄_clean.pdf
UMCDOJ-06920267	201712_201811_PM member list.xlsx
UMCDOJ-06920269	F32 Document Sharing List-2018.xlsx
UMCDOJ-06920275	R20185365.pdf
UMCDOJ-06920276	R20185366.pdf
UMCDOJ-06920277	R20185367.pdf
UMCDOJ-06920278	R20185368.pdf
UMCDOJ-06920279	TD information security policy.pptx
UMCDOJ-06920280	[NBDO Document Library] DRAM F32 Documents Sharing with JHICC .pdf
UMCDOJ-06920281	劳动合同_何建廷_08012016.doc
UMCDOJ-06920283	劳动合同_李甫哲_08012016.doc
UMCDOJ-06920288	劳动合同_郭峰銘_08012016.doc
UMCDOJ-06920293	顧問聘用合同_01-16李甫哲-20160708拓维修订稿.docx
UMCDOJ-06920298	顧問聘用合同_02-16郭峰銘-20160708拓维修订稿.docx

Exhibit 1-30

UMCDOJ-06920303	⑧Pj SA1 Design Review_Rev.1.0.pdf
UMCDOJ-06920308	Project M Process Flow @ 0922 2016_DRAM ⑧p⑧bl⑧. pptx
UMCDOJTT-00002369	Micron DDR3 to DDR4-internal net download-.pdf
UMCDOJTT-00029513	
UMCDOJTT-00080306	
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USD-0000308	
USD-0000654	
USD-0000657	"Re Presentation Materials for PPG (Etch, DCVD, ALD, SRP).msg"
USD-0000695	.msg
USD-0003644	UMC Executive Meeting TIG (25 Oct'16).pdf
USD-0003649	APTD Overview by Dr Ping.msg
USD-0003650	DRAM and APTD Overview (24 Oct'16) Dr Ping.pdf
USD-0003747	jhicc cta 20180201.pdf
USD-0003748	re: umc project m meeting minutes.msg
USD-0003928	Etch PSE list 2016_05.xlsx
USD-0003971	re: umc proj m dram low 6/13/16.msg
USD-0003973	UMC DRAM Project M_Update_0613_V11.pptx
USD-0003979	acr materials_ver4.msg
USD-0003980	UMC_ACR_Jul2016_rev4.pptx
USD-0004003	re: caspa: speech at caspa summer mixer on august 26, 2016 - jinhua.msg
USD-0004004	China DRAM.pptx
USD-0004946	re: caspa: speech at caspa summer mixer on august 26, 2016 - jinhua.msg
USD-0004951	China DRAM.pptx
USD-0004961	jhicc meeting minutes - march 2, 2017.msg
USD-0004966	20180601_PO (AMAT)_采购总监签核.pdf
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Exhibit 1-31

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Exhibit 1-32

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USD-0885695	

**Exhibit 2: Selected Documents and Information Requested of UMC
under Paragraph 9 of the Plea Agreement signed October 26, 2020**

- United Microelectronics Corporation, Inc. ("UMC") board of directors packages, presentations, minutes, and other information considered by the directors of UMC for the calendar quarters from the third quarter of 2015 to the fourth quarter of 2019, as follows –
 - All documents and information for the third and fourth quarters of 2015 and the four quarters of calendar year 2016;
 - Extracts of documents for the calendar quarters of 2017, 2018, and 2019 that in any way refer or relate to Project M, DRAM, memory chips, Fujian Jinhua, or the Cooperation Agreement referenced in paragraph 2(j) of the plea agreement;
 - The date range refers to quarterly reporting periods and the requested documents may have been sent before or after the relevant quarter
 - for example, a board of directors meeting in respect of a calendar quarter may take place after the conclusion of that quarter
 - documents and information should be produced if they relate to the quarter even if the documents bear dates outside the quarter
- To the extent not already produced from custodial files, UMC's discussions with possible external business partners in China and the Cooperation Agreement referenced in paragraph 2(g) and (j) of the plea agreement; with respect to the Cooperation Agreement, this request includes but is not limited to
 - The negotiating history of the Cooperation Agreement
 - Drafts and revisions of the Cooperation Agreement
 - Due diligence checklists and due diligence documents related to execution of the Cooperation Agreement, including the formation and funding of Fujian Jinhua
- To the extent not already produced from custodial files, UMC's efforts to develop DRAM technology, variously referred to as the Project in paragraph 2 of the plea agreement, Project M, New Business Development, and by any other name, including but not limited to
 - Project approval and management (e.g., investment analysis, business plans, project schedules, and organization charts)
 - Source of DRAM process technology and memory product design (e.g., reference logic process flows, public domain libraries and share files, reverse engineering analysis, licenses or other IP contracts, product designs, enumeration of new IP blocks developed exclusively for DRAM or licensed (such as from Cadence or Synopsys), sources of IP, block by block, with accompanying commercial agreements, and mask house and packaging and test partners used)

Exhibit 2-2

- Technology development plan (e.g., Product Requirements Document, reference UMC process technology, methodology and details for the derivation of the initial DRAM process flow, gap analysis between UMC reference process and target DRAM process, process design kit (PDK), schedule / timeline with test chips, cycles, and shuttles, Stage Gates with exit criteria, and Design of Experiments plan)
- Resource plan (e.g., detailed operating budget, headcount, recruiting, manpower curve, and R&D capacity and facility resources)
- New tool acquisition (e.g., selection process, rationale, cost and schedule for each new tool, and total capital expenditure budget)
- Risk and mitigation plan (e.g., market, technology, schedule, business, and political)
- Program governance (e.g., periodic management reports and progress reviews within UMC and to Fujian Jinhua)
- List of UMC employees on Project M with their UMC employee numbers.

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Exhibit 3: Summary of Information Terrence Daly Received in Video Conferences with Micron Employees

A series of nine horizontal black bars of varying lengths, arranged vertically. The bars are thick and solid black, with some showing slight texture or noise. They are positioned against a white background.

CONFIDENTIAL – SUBJECT TO PROTECTIVE ORDER

Exhibit 3-2

The image consists of nine horizontal black bars of varying lengths, arranged vertically. Each bar has a small white rectangular notch cut out of its right edge. The bars are set against a white background.

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Exhibit 3-3

Digitized by srujanika@gmail.com

1. *What is the primary purpose of the study?*

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Exhibit 3-4

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For more information, contact the Office of the Vice President for Research and Economic Development at 515-294-6450 or research@iastate.edu.

A dark, textured surface, likely a book cover or endpaper, showing vertical grain and some wear along the edges.

100

A dark, textured surface, likely a book cover or endpaper, showing signs of wear and discoloration. The left edge reveals the binding structure.

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Exhibit 3-5

CONFIDENTIAL – SUBJECT TO PROTECTIVE ORDER

Exhibit 3-6

Exhibit 4: Summary of Video Conference between Terrence Daly and Thomas Dyer on March 4, 2021

Mr. Daly asked Dr. Dyer from a technical perspective whether a link exists between the cell array (e.g., 2x3 or 3x2) and manufacturing process. Dr. Dyer answered that they are linked and that the three leading DRAM manufacturers moved from a 2x3 to a 3x2 cell array to minimize row hammer effect.

Mr. Daly asked Dr. Dyer about the source of the DRAM manufacturing process steps, recipes, and tools in the minutes of the December 7, 2015 meeting. Dr. Dyer answered that the steps, their order, the recipes, and the tools appear to be identical to the same information in certain Micron travelers. Dr. Dyer also explained that E300 and R1 are the former names of the Elpida (Japan) and Rexchip (Taiwan) fabs, respectively, which are now Micron's F15 and F16 fabs.

Mr. Daly asked if UMC could have developed a DRAM process technology solely from the combination of: (a) established logic flows, (b) TRENDFORCE analysis, (c) UMC reverse engineering (TEM/SEM analysis), (d) equipment vendor input and support, (e) hiring experienced DRAM engineers, and (f) blocking and tackling of R&D with test sites, short loops, DOEs, etc. Mr. Daly's preliminary view was that development was conceivable, but not at the speed or with the thin resources evident in UMC documents from December 2015 through December 2016. Dr. Dyer's preliminary view was that development was not feasible in the Project M timeframe. Dr. Dyer explained that DRAM is different than logic, that the memory cell and array designs are highly evolved over successive technology generations, and that unique processes (e.g., buried word-lines into the substrate, stacked capacitors) would be required for a logic foundry.

Mr. Daly asked what is "BM2"? Dr. Dyer answered that "BM" typically means "benchmark."

Mr. Daly asked whether PDKs are used by DRAM manufacturers. Dr. Dyer answered that logic foundries use PDKs but DRAM IDM's do not have formal PDKs.

Messrs. Daly and Dyer discussed the role of UMI. Dr. Dyer explained the "GDS," which is a layer-by-layer definition of the chip design.

